IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: FRANCIS ET AL.

Examiner: T. LEE

Serial No. 10/008,586

Art Unit: 2115

Filing Date: NOVEMBER 5, 2001

Attorney Docket No. 53314

For: DEVICE AND METHOD FOR

SELECTIVELY POWERING DOWN INTEGRATED CIRCUIT BLOCKS WITHIN A SYSTEM ON CHIP

STATUS REQUEST

RECEIVED MAY 0 6 2004

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 Technology Center 2100

Sir:

MAY 0 3 2004

Applicants request the status of the above identified patent application, which was filed on November 5, 2001. filing receipt, Notice to File Missing Parts, recorded Assignment and Notice of Publication have been received but there has been no further communication from the U.S. Patent and Trademark Office regarding this application.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29th day of April, 2004.